1. A method for performing time slot switching of synchronous data across an asynchronous medium comprising:

(a) converting synchronous serial data related to a source time slot into synchronous parallel data units in accordance with a synchronous clock signal;

(b) formatting the synchronous parallel data units into a first subpacket in accordance with the synchronous clock signal, the first subpacket generated during a first synchronization interval of the synchronous clock signal;

(c) generating a packet from a plurality of subpackets, including the first subpacket;

(d) asynchronously transmitting the packet across an asynchronous medium; and

(e) extracting the subpackets from the packet and storing the subpackets in a plurality of buffers, each of the buffers associated with a destination time slot,

the arrangement of subpackets within the buffers being determined by the first synchronization interval during which the subpacket was generated plus a fixed delay offset.

2. An apparatus for performing time slot switching of synchronous data across an asynchronous medium comprising:

(a) serial to parallel interface for converting synchronous serial data related to a source time slot into synchronous parallel data units in accordance with a synchronous clock signal;

(b) logic for formatting the synchronous parallel data units into a first subpacket in accordance with the synchronous clock signal, the first subpacket generated during a first synchronization interval of the synchronous clock signal;

(c) logic for generating a packet from a plurality of subpackets, including the first subpacket;

(d) logic for asynchronously transmitting the packet across an asynchronous medium;

(e) logic for extracting the subpackets from the packet and for storing the subpackets into a plurality of buffers, each of the buffers associated with a destination time slot,

the arrangement of subpackets within the buffers being determined by a value representing the first synchronization interval plus a fixed delay offset.

3. A method for transferring data comprising:

(a) packetizing a plurality of synchronous serial data streams into respective subpackets during a first synchronization interval, each subpacket associated with a source time slot;

(b) asynchronously transmitting the subpackets through an asynchronous medium; and

(c) reconverting the subpackets into synchronous data streams during a second synchronization interval having a fixed delay offset relation to the first synchronization interval.

4. The method of claim 3 wherein (a) comprises:

(a1) converting the synchronous serial data streams into synchronous parallel data units.

5. The method of claim 4 wherein (a) comprises:

(a2) formatting the synchronous parallel data units into a subpackets during a first synchronization interval.

6. The method of claim 5 wherein (b) comprises:

(b1) generating a packet from a plurality of subpackets,

the packet including data identifying the first synchronization interval during which the subpackets were formatted from the synchronous parallel data units, and a destination time slot identifier associated with each subpacket.

7. The method of claim 6 wherein (b) comprises:

(b2) asynchronously transmitting the subpackets through an asynchronous medium as part of the packet.

8. The method of claim 3 wherein (c) comprises:

(c1) extracting the subpackets from the packet, and

(c2) storing the subpackets into a plurality of buffers, each of the buffers associated with a destination time slot, the arrangement of subpackets within the buffers being determined by a value representing the first synchronization interval plus a fixed delay offset.

9. The method of claim 8 wherein (c) comprises:

(c3) reading the subpackets from the buffers as a plurality of parallel data units; and

(c4) converting the parallel data units into synchronous serial data streams.

10. A apparatus for transferring data comprising:

(a) a source of synchronization signals defining a plurality synchronization intervals;

(b) an interface for packetizing a plurality of synchronous data streams into respective subpackets during a first synchronization interval, each subpacket associated with a source time slot;

(c) a mechanism for asynchronously transmitting the subpackets through an asynchronous medium; and

(d) an interface for reformatting the subpackets into synchronous data streams during a second synchronization interval having a fixed delay offset relation to the first synchronization interval.

11. The apparatus of claim 10 wherein (b) comprises:

(b1) logic for converting the synchronous serial data streams into synchronous parallel data units.

12. The apparatus claim 11 wherein (b) comprises:

(b2) logic for formatting the synchronous parallel data units into a subpackets during a first synchronization interval.

13. The apparatus of claim 12 wherein (b) comprises:

(b3) logic for generating a packet from a plurality of subpackets,

the packet including data identifying the first synchronization interval during which the subpackets were formatted from the synchronous parallel data units, and a destination time slot identifier associated with each subpacket.

14. The apparatus of claim 13 wherein (c) comprises an asynchronous switch.

15. The apparatus of claim 10 wherein (d) comprises:

(d1) logic for extracting the subpackets from the packet, and

(d2) logic for storing the subpackets into a plurality of buffers, each of the buffers associated with a destination time slot, the arrangement of subpackets within the buffers being determined by a value representing the first synchronization interval plus a fixed delay offset.

16. The apparatus of claim 15 wherein (d) comprises:

(d3) logic for reading the subpackets from the buffers as a plurality of parallel data units; and

(d4) logic for converting the parallel data units into synchronous serial data streams.

17. An apparatus comprising:

(a) an asynchronous switch;

(b) a plurality of circuit server modules coupled to the asynchronous switch, the server modules comprising:

(i) a time division multiplex interface; and

(ii) data adaptation logic; and

(c) a source of synchronous clock signals coupled to each of the circuit server modules, the synchronous clock signals defining a plurality of synchronization intervals;

the circuit server modules configured to perform synchronous time slot switching of synchronous data across the asynchronous switch.

18. The apparatus of claim 17 wherein the time division multiplex interface comprises:

serial to parallel conversion logic for converting synchronous serial data streams into parallel data units.

19. The apparatus of claim 17 further comprising:

parallel-to-serial conversion logic for converting a plurality of parallel data units into synchronous serial data streams.

20. The apparatus of claim 18 wherein the data adaptation layer comprises:

an ingress data memory coupled to the time division multiplexed interface;

an ingress context memory; and

subpacket construction logic for constructing in the ingress data memory a plurality of subpackets during one of the synchronization intervals, each subpacket associated with a source time slot and containing parallel data derived from a synchronous serial data stream received through the time division multiplexed interface subpacket.

21. The apparatus of claim 20 wherein the ingress context memory stores context data associated with a subpacket, the context data comprising a destination time slot identifier and a queue identifier associated with a subpacket.

22. The apparatus of claim 21 wherein the data adaptation layer comprises:

an ingress queue coupled to the asynchronous switch; and

packet construction logic for constructing in the ingress queue a packet including a plurality of subpackets and the respective context data associated with each subpacket.

23. The apparatus of claim 22 wherein the packet further comprises data identifying the synchronization interval during which the subpackets contained therein were constructed.

24. The apparatus of claim 17 wherein the data adaptation layer further comprises:

an egress data memory having a plurality of playout buffers associated with a plurality of destination time slots; and

depacketizing logic for receiving a packet form the asynchronous switch and for storing subpackets contained therein into the plurality of playout buffers in the egress data memory.

25. The apparatus of claim 24 wherein the data adaptation layer further comprises:

playout logic for synchronously supplying parallel data from the playout buffers to the time division multiplexed interface.

26. A memory for storing data to be processed by a data processing system including an asynchronous switch, the memory comprising:

a data structure stored in the memory and usable to perform time slot switching of data, the data structure comprising:

a plurality of subpackets, each subpacket associated with a source time slot and containing parallel data derived from a synchronous serial data stream, each subpacket constructed during a common synchronization interval;

a synchronization tag identifying the common synchronization interval during which the plurality of subpackets were constructed;

data identifying the number of subpackets contained within the data structure; and

context data associated with each one of the plurality of subpackets, the context data including a destination time slot identifier corresponding to the source time slot associated with a subpacket.